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;Demonstrate full H-bridge PWM output.  (fixed frequency/variable duty cycle)
;PWM output = 4kHz
;************************PIN ASSIGNMENTS:**************************************
;PORTC, 2 (P1A) = Upper right MOSFET
;PORTD, 5 (P1B) = Lower right MOSFET
;PORTD, 6 (P1C) = Upper left MOSFET
;PORTD, 7 (P1D) = Lower left MOSFET
;PORTA, 0/ANO = potentiometer (analog input)

   list            p=16f1937     ;list directive to define processor
   #include     <p16f1937.inc>                ; processor specific variable definitions

   errorlevel -302       ;no "register not in bank 0" warnings
   errorlevel -312     ;no  "page or bank selection not needed" messages

   #define BANK0  (h'000')
   #define BANK1  (h'080')
   #define BANK2  (h'100')
   #define BANK3  (h'180')

   __CONFIG _CONFIG1,    _MCLRE_OFF & _CP_OFF & _CPD_OFF & _BOREN_OFF &
_WDTE_OFF & _PWRTE_ON & _FOSC_INTOSC & _FCMEN_OFF & _IESO_OFF

;Context saving variables:
CONTEXT     UDATA_SHR
w_temp                  RES    1         ; variable used for context saving

;General Variables
GENVAR       UDATA

;*****************************************************************************
   ORG                  0x000
   pagesel              start     ; processor reset vector
   goto          start     ; go to beginning of program
INT_VECTOR:
   ORG                  0x004           ; interrupt vector location
INTERRUPT:

start:


   banksel BANK1
   ;Set PORTS to output
   movlw   b'00000001'
   movwf   (TRISA ^ BANK1)
   movlw   b'00000000'                  ;PORTB <6:7> = input 2, 1 on L293D
   movwf   (TRISB ^ BANK1)
   movlw   b'00000000'                  ;PORTC, 2=CCP1/P1A
   movwf   (TRISC ^ BANK1)
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movlw   b'00000000'
movwf   (TRISD ^ BANK1)
movlw   b'00000000'
movwf   (TRISE ^ BANK1)

;Config ADC:
movlw   b'00000001' ;Pin AN0/PORTA, 0 configured as analog input
banksel ANSELA
movwf   ANSELA

movlw   b'00010000'
        ;0-------  ADFM=0 (left justified. 8MSBs are in ADRESH
        ;-001----  ADCS<0:2>, bits 4-6 =001. (2.0uS)
                   ;FOSC/8=4Mhz/8 (doubles instruction cycle time)
                   ;Instruction Cycle period (TCY) now equals
                   ;2uS (greater than 1.6uS necessary for ADC)
banksel ADCON1
movwf   ADCON1

movlw   b'00000001'
        ;-00000--   CHS<0:4> (bits 2-6) = 00000 = pin AN0)/PORTA, 0 as analog input
        ;------0-  Stop AD conversion
        ;-------1  Enable ADC
banksel ADCON0
movwf   ADCON0

movlw   b'01101000'
banksel OSCCON  ;Set processor clock to 4mHz (not really necessary as its the default setting)
movwf   OSCCON
;***************Configure PWM*********************************************
;TMR2
movlw   b'00000101'    ; configure Timer2:
      ; -----1--      turn Timer2 on (TMR2ON = 1)
      ; ------01      prescale = 1:4 (T2CKPS = 01)
banksel T2CON          ;TMR2 increments every 4 us
movwf   T2CON
;Load 255 into PR2
movlw   .255           ;period = 1024uS = 1mS = 977 Hz
banksel PR2
movwf   PR2
;Configure CCP1 to be based off of TMR2:
banksel CCPTMRS0
movlw   b'11111100'
movwf   CCPTMRS0          ;bits 0:1=0=TMR2 for CCP1

movlw   b'01001110'
        ;01------  Full-bridge output forward (P1D modulated, P1A active,
                   ;P1B/P1C inactive
        ;--00----  DC1B=00 (2 LSB's of PWM duty cycle=00)
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            ;----1110  PWM mode :P1A, P1C active-low
                                ;P1B, P1D active-high (CCP1M=1110)
   banksel CCP1CON
   movwf   CCP1CON
   ;Dead-band delay:
   movlw   b'0111111'
   banksel PWM1CON
   movwf   PWM1CON

mainLoop
   ;Sample analog input:
   banksel         ADCON0
   bsf             ADCON0, GO
waitADC
   btfsc   ADCON0, NOT_DONE
   goto    waitADC

   ;Determine motor direction:
   banksel         ADRESH
   btfss   ADRESH, 7           ;MSB of ADRESH determines direction
   goto    mtrReverse    ;1=forward, 0=reverse

   ;FORWARD MODE:

   ;1) set new duty cycle:
   rlf             ADRESH, w
   banksel         CCPR1L      ;PWM duty cycle =
   movwf           CCPR1L      ;(high byte of ADC result-128) / 128

   ;2) select forward mode:
   banksel         CCP1CON     ;select full-bridge output forward (P1M<1> = 0)
   bcf             CCP1CON, P1M1   ;P1D modulated
                               ;P1A active (low)
                               ;P1B inactive (low)
                               ;P1C inactive (high)
   goto    mainLoop

   ;REVERSE MODE
mtrReverse
   ;1) Set new duty cycle:
   banksel         ADRESH
   comf            ADRESH, f   ;ADRESH = 255 - ADRESH
   rlf             ADRESH, w
   banksel         CCPR1L      ;PWM duty cycle =
   movwf           CCPR1L      ;(127-ADRESH) / 128

   ;2) Select reverse mode:
   banksel         CCP1CON     ;select full-bridge reverse (P1M<1> = 1)
   bsf             CCP1CON, P1M1   ;P1B modulated (active-high)
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                        ;P1C active (low)
                        ;P1A inactive (high)
                        ;P1D inactive (low)
goto    mainLoop

END
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